



Statement of Volatility – Dell DX6104-CSN and DX6104-SN

Dell DX6104-CSN and DX6104-SN systems contain both volatile and non-volatile (NV) components. Volatile components lose their data immediately upon removal of power from the component. Non-volatile components continue to retain their data even after the power has been removed from the component. Components chosen as user-definable configuration options (those not soldered to the motherboard) are not included in the Statement of Volatility. Configuration option information (pertinent to options such as microprocessors, remote access controllers, and storage controllers) is available by component separately. The following NV components are present in the DX6104-CSN and DX6104-SN systems.

Item	Non-Volatile or Volatile	Quantity	Reference Designator	Size
Planer				
PCH Internal CMOS RAM	Non-Volatile	1	U39	256 Bytes
BIOS SPI Flash	Non-Volatile	1	U4-1	8 MB
iDRAC SPI Flash	Non-Volatile	1	U22-1	4 MB
BMC EMMC	Non-Volatile	1	U45	2 GB
System CPLD RAM	Volatile	1	U19	8kb
System Memory	Volatile	Up to 6 per CPU	CPU1: DIMM1~DIMM6, CPU2: DIMM7~DIMM12	Up to 32GB per DIMM
Power Supplies				
PSU FW	Non-Volatile	1 per PSU	Varies by part number	Up to 2MB. Varies by part number
4x3.5" Backplane				
SEP internal flash	Non-Volatile	1	U_SEP	Flash:32KB + 4KB EEPROM: 1KB

8x2.5" Backplane				
SEP internal flash	Non-Volatile	1	U3(SEP)	Flash:32KB + 4KB EEPROM: 1KB

Item	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)
Planer			
PCH Internal CMOS RAM	Battery-backed CMOS RAM	No	Real-time clock and BIOS configuration settings
BIOS SPI Flash	SPI Flash	YES	Boot code, system configuration information, UEFI environment, Flash Disceptor, ME
iDRAC SPI Flash	SPI Flash	No	iDRAC Uboot (bootloader), server management persistent store (i.e. iDRAC MAC Address, iDRAC boot variables), lifecycle log cache, virtual planar FRU and EPPID, rac log, System Event Log, JobStore, iDRAC Secure Boot Code,
BMC EMMC	eMMC NAND Flash	No	Operational iDRAC FW, Lifecycle Controller (LC) USC partition, LC service diags, LC OS drivers, USC firmware
CPU Vcore and VSA Regulators	OTP(one time programmable)	No	Operational parameters
System CPLD RAM	RAM	No	Not utilized
System Memory	RAM	Yes	System OS RAM
Power Supplies			
PSU FW	Embedded microcontroller flash	No	Power Supply operation, power management data


			and fault behaviors
4x3.5" Backplane			
SEP internal flash	Integrated Flash+EEPROM	No	Firmware + FRU
8x2.5" Backplane			
SEP internal flash	Integrated Flash+EEPROM	No	Firmware + FRU

Item	How is data input to this memory?	How is this memory write protected?
Planer		
PCH Internal CMOS RAM	BIOS	N/A – BIOS only control
BIOS SPI Flash	SPI interface via iDRAC	Software write protected
iDRAC SPI Flash	SPI interface via iDRAC	Embedded iDRAC subsystem firmware actively controls sub area based write protection as needed.
BMC EMMC	NAND Flash interface via iDRAC	Embedded FW write protected
CPU Vcore and VSA Regulators	Once values are loaded into register space a cmd writes to nvm.	There are passwords for different sections of the register space
System CPLD RAM	Not utilized	Not accessible
System Memory	System OS	OS Control
Power Supplies		
PSU FW	Different vendors have different utilities and tools to load the data to memory. It can also be loaded by Dell Update Package from LC or OS (Windows and Linux)	Protected by the embedded microcontroller. Special keys are used by special vendor provided utilities to unlock the ROM with various CRC checks during load.
4x3.5" Backplane		
SEP internal flash	I2C interface via iDRAC	Program write protect bit
8x2.5" Backplane		
SEP internal flash	I2C interface via iDRAC	Program write protect bit

Item	How is this memory write protected?	How is the memory cleared?
Planer		
PCH Internal CMOS RAM	N/A – BIOS only control	1) Set NVRAM_CLR jumper to clear BIOS configuration settings at boot and reboot system; 2) AC power off system, remove coin cell battery for 30 seconds, replace battery and power back on; 3) restore default configuration in F2 system setup menu.
BIOS SPI Flash	Software write protected	Not possible with any utilities or applications and system is not functional if corrupted/removed.
iDRAC SPI Flash	Embedded iDRAC subsystem firmware actively controls sub area based write protection as needed.	Not completely user clearable; however, user data, lifecycle log and archive, SEL, fw image repository can be cleared via Delete Configuration and Retire System, accessible in Lifecycle Controller interface
BMC EMMC	Embedded FW write protected	Not completely user clearable; however, user data, lifecycle log and archive, SEL, fw image repository can be cleared via Delete Configuration and Retire System, accessible in Lifecycle Controller interface
CPU Vcore and VSA Regulators	There are passwords for different sections of the register space	Not user clearable
System CPLD RAM	Not accessible	Not accessible
System Memory	OS Control	Reboot or power down system
Internal USB Key	No write protect	Can be cleared in system OS
Trusted Platform Module (TPM)	SW write protected	F2 Setup option
Power Supplies		
PSU FW	Protected by the embedded microcontroller. Special keys are used by special vendor provided utilities to unlock the ROM with various CRC checks during load.	Not clearable
8x2.5" Backplane		
SEP internal flash	Program write protect bit	Not user clearable

2x2.5" Backplane		
SEP internal flash	Program write protect bit	Not user clearable
24x2.5" Backplane		
Flash memory	Hardware strapping	Not user clearable
Expander FRU image	Hardware strapping	Not user clearable
BP FRU image	Hardware strapping	Not user clearable
16x2.5" Backplane		
Flash memory	Hardware strapping	Not user clearable
Expander FRU image	Hardware strapping	Not user clearable
BP FRU image	Hardware strapping	Not user clearable
8x3.5" Backplane		
SEP internal flash	Program write protect bit	Not user clearable
12x3.5" Backplane		
Flash memory	Hardware strapping	Not user clearable
BP FRU image	Hardware strapping	Not user clearable
Expander FRU image	Hardware strapping	Not user clearable
PCIe SSD Backplane		
SEP internal flash	Program write protect bit	Not user clearable
H710, H810, H710M PERCs		
NVSRAM	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer
FRU	Not WP	Cannot be cleared with existing tools available to the customer
1-Wire EEPROM	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer
SPD	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer
SBR	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer
SPI Flash	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer
Flash	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer

ONFI Backup Flash	Not WP. Not visible to Host Processor	Flash can be cleared by powering up the card and allowing the controller to flush the contents to VD's. If the VD's are no longer available, cache can be cleared by going into controller bios and selecting Discard Preserved Cache.
SDRAM	Not WP. Not visible to Host Processor	Cache can be cleared by powering off the card
H310, H310M PERCs		
NVSRAM	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer
FRU	Not WP	Cannot be cleared with existing tools available to the customer
1-Wire EEPROM	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer
SBR	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer
Flash	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer
PCIe SSD Extension Card		
Switch Configuration EEPROM	Device can be write protected via hardware pin. Alternatively, device contents can be write protected via WPEN bit in status register.	System is not functional as intended if corrupted/removed.
IDSDM		
SPI Flash	Hardware strapping	Not user clearable
MCU	N/A	Not user clearable

 **NOTE:** For any information that you may need, direct your questions to your Dell Marketing contact.

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